

# MS7301 Version:0A

TITLE	SHEET
COVER SHEET	1
BLOCK DIAGRAM	2
PWR MAP/CLOCK MAP	3
GPIO/MEMORY/PCI/HW STRPPING	4
PROCESSOR (LGA775)	5-7
NORTH BRIDGE P4M890	8-11
SOUTH BRIDGE VT8237A	12-14
CLOCK GEN. & Buffer	15
SYS MEM-DDRII	16
PCI-Express Slot x16 / x1	17
PCI 1 & 2	18
Audio - ALC883	19
LAN-VT6103L	20
SATA RAID VT6421	21
IDE & SATA	22
USB-REAR & FRONT	23
1394-VT6307 COLAY VT6308P	24
LPC IO-W83627EHG & BIOS	25
KB/MS & FAN & VGA	26
VRM- Intersil 6312	27
MS7 ACPI CONTROLLER	28
BULK/Decopuling/ATX POWER CONNECTOR / FRONT PANEL	29
<b>HISTORY</b>	30
Manual Part	31

## CPU:

Intel LGA775

## System Chipset:

PT890/P4M900 (North Bridge)  
VT8237A (South Bridge)

## On Board Chipset:

BIOS -- LPC ROM  
Audio - ALC883  
LPC Super I/O -- W83627EHG  
LAN --VT6103L  
CLOCK --ICS9LPR700AGLF

## Main Memory:

single-channel --DDRII\*2

## Expansion Slots:

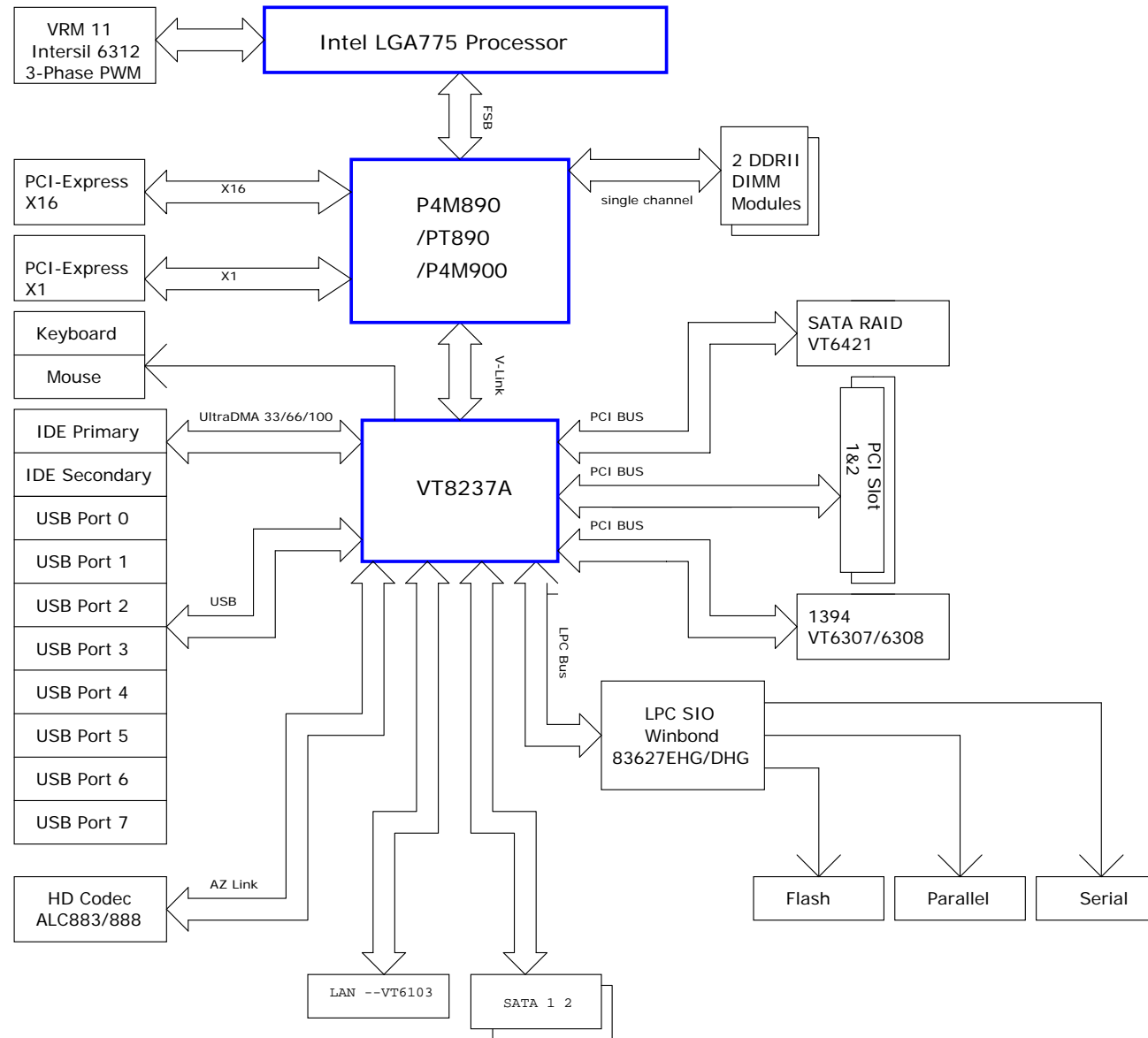
PCI Express X16 \* 1  
PCI Express X1 \* 1  
PCI 2.2Slot \* 2

## PWM(VRM11/FMB 05B):

Intersil 6312

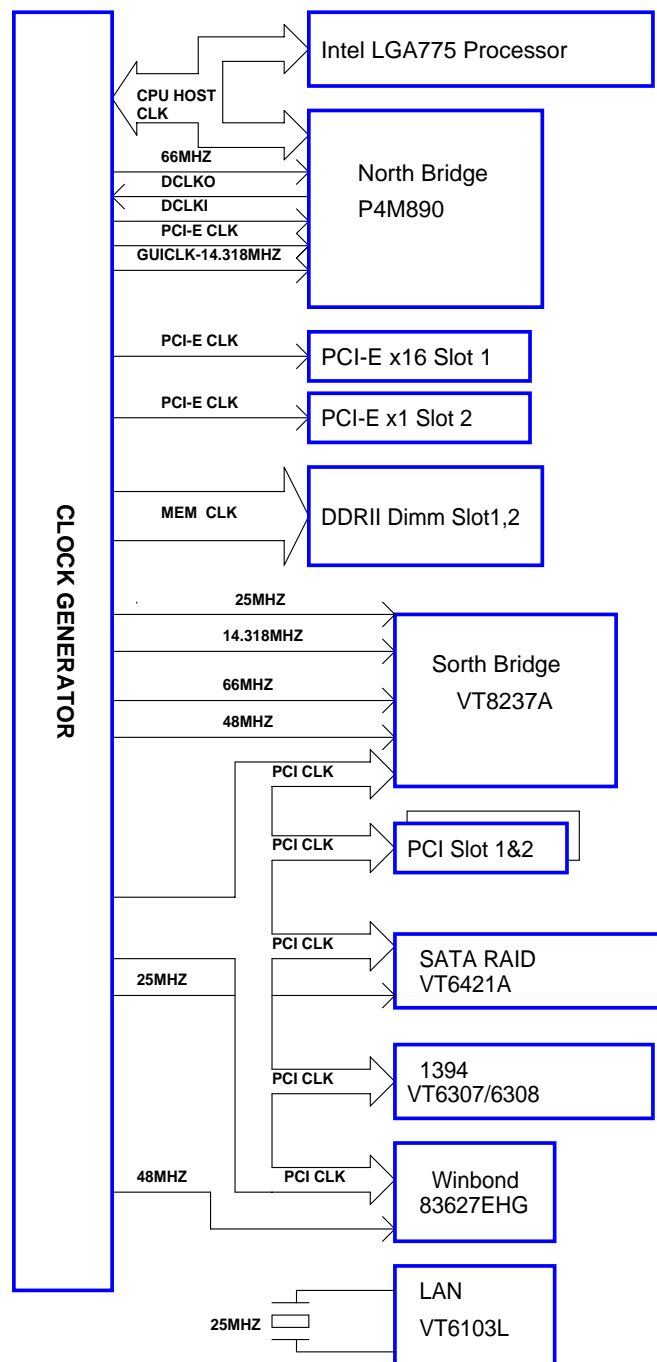
Micro Star Restricted Secret	
Title	Rev
COVER SHEET	0A
Document Number	MS-7301
MICRO-STAR INT'L CO., LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan <a href="http://www.msi.com.tw">http://www.msi.com.tw</a>	
Last Revision Date: Tuesday, April 11, 2006	
Sheet	1 of 31

# Block Diagram

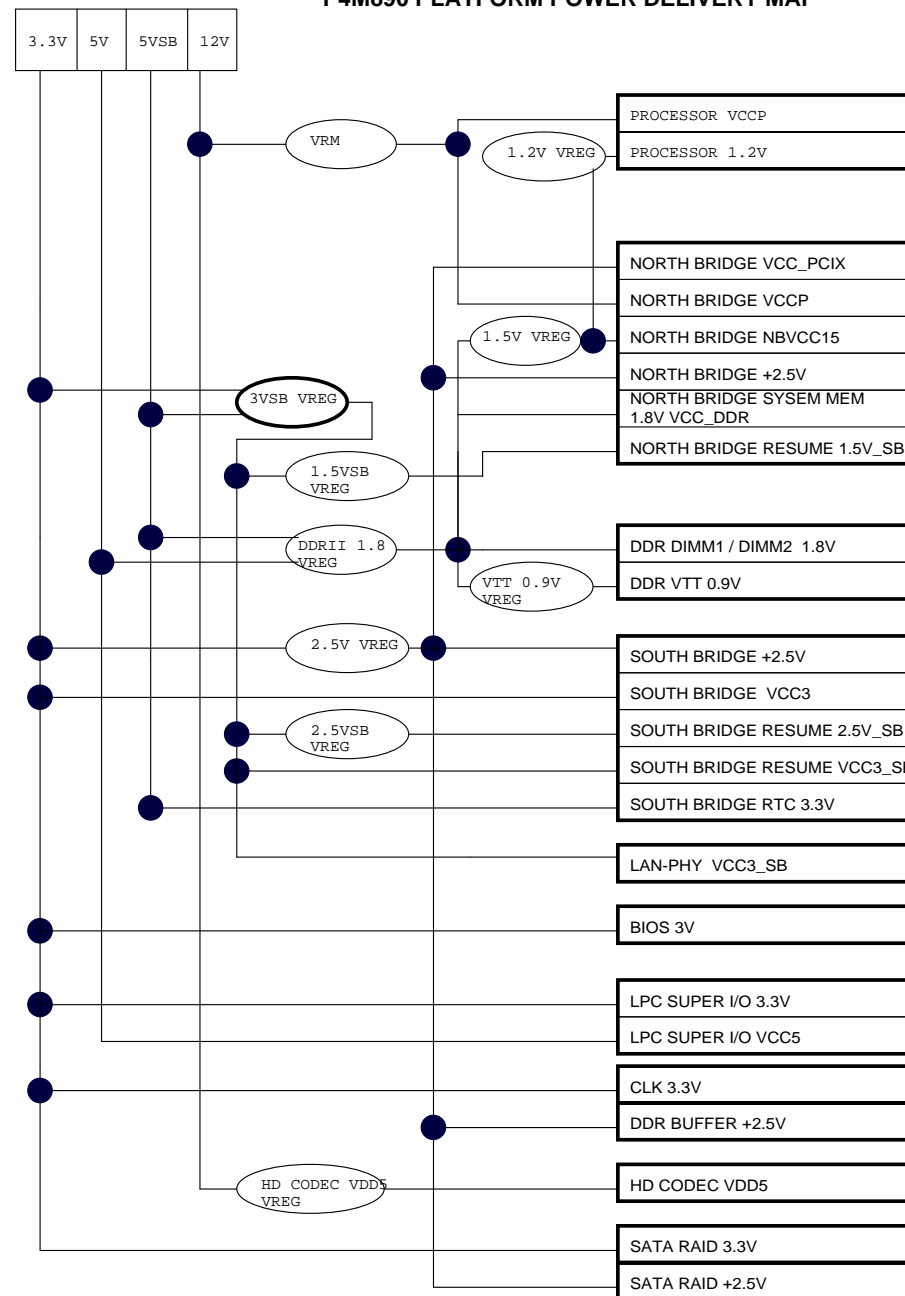


Micro Star Restricted Secret		
Title	BLOCK DIAGRAM	Rev 0A
Document Number	MS-7301	
MICRO-STAR INT'L CO., LTD. No. 69, Li-De St, Jung-Ho City, Taipei Hsien, Taiwan <a href="http://www.msi.com.tw">http://www.msi.com.tw</a>		Last Revision Date: Tuesday, April 11, 2006 Sheet 2 of 31

P4M890 PLATFORM CLOCK GENERATOR MAP



P4M890 PLATFORM POWER DELIVERY MAP



Micro Star Restricted Secret

Title	Rev
PWR AND CLOCK MAP	
Document Number	MS-7301
0A	

MICRO-STAR INT'L CO., LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan <a href="http://www.msi.com.tw">http://www.msi.com.tw</a>	Last Revision Date: Tuesday, April 11, 2006 Sheet 3 of 31
--	---

### SB-VT8237A

GPIO Pin	Type	Function	Power well
GPI 0	I	GPI 0	RESUME
GPI 1	I	SB_THERMTRIP#	RESUME
GPO 0	O	FAN_CTRL1	RESUME
GPO 1	O	FAN_CTRL	RESUME
GPIO A	I/O	Vlink auto compensation	MAIN
GPIO B	I/O	IOQ Depth	MAIN
GPIO C	I/O	HOST CLOCK	MAIN
GPIO D	I/O	GTL pullup	MAIN

### DDR DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1	1010000B	MDCLKA0/A#0 MDCLKA1/A#1 MDCLKA2/A#2
DIMM 2	1010001B	MDCLKB0/B#0 MDCLKB1/B#1 MDCLKB2/B#2

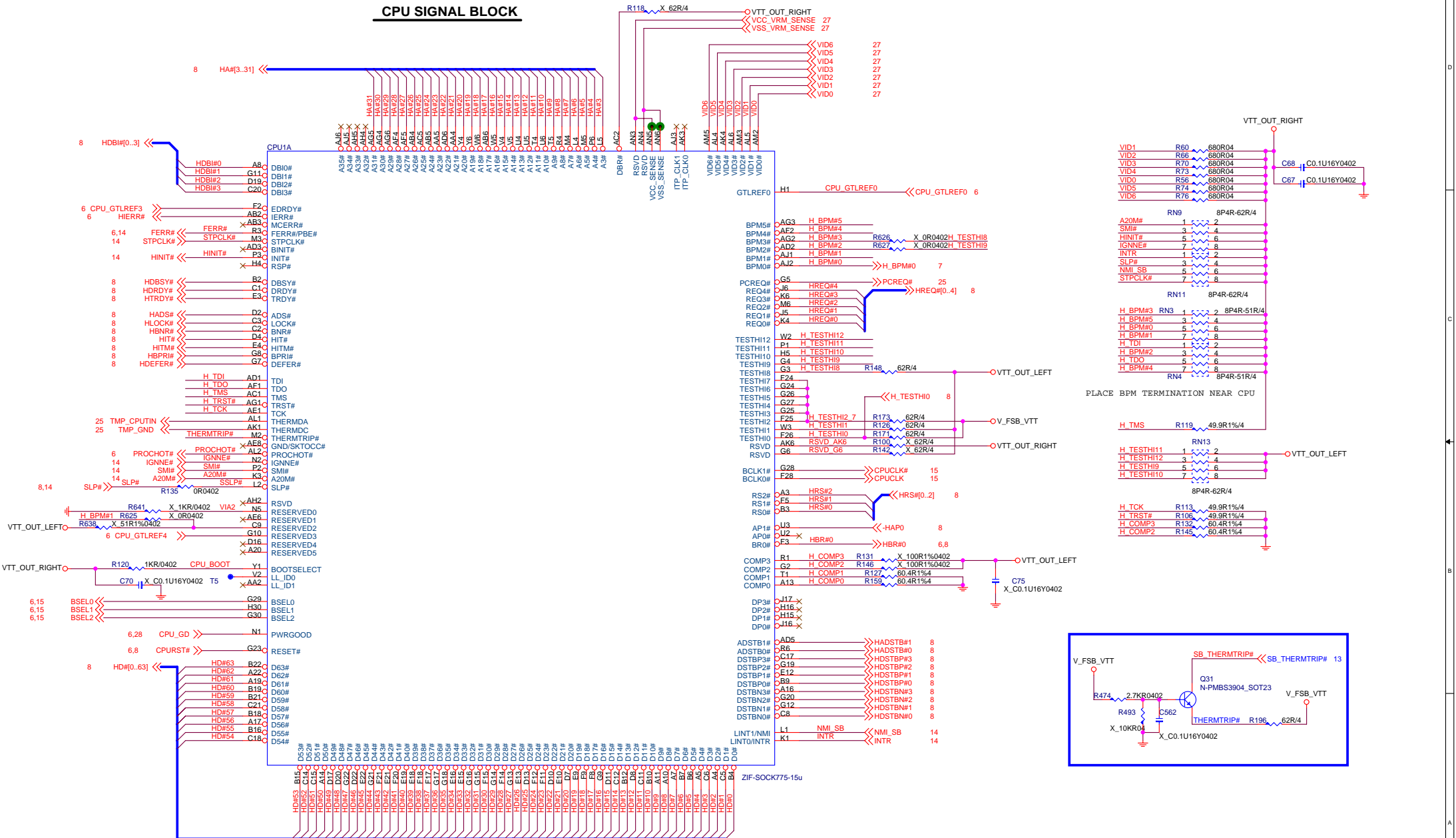
### PCI Config.

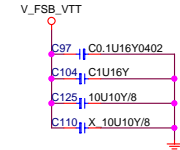
DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK	CLK GEN PIN OUT
PCI Slot 1	PIRQ#A PIRQ#B PIRQ#C PIRQ#D	PREQ#0 PGNT#0	AD20	PCICLK1	5 (PCI_CLK2)
PCI Slot 2	PIRQ#B PIRQ#C PIRQ#D PIRQ#A	PREQ#1 PGNT#1	AD21	PCICLK2	6 (PCI_CLK3)
SATA RAID	PIRQ#E	PREQ#2 PGNT#2	AD22	SATA_PCLK	7 (PCI_CLK4)
1394	PIRQ#F	PREQ#3 PGNT#3	AD19	1394_PCLK	1 (PCI_CLK1)

### PCI RESET DEVICE

Signals	Source	Target
PCIRST#	SB	MS7
PCIRST#1	MS7	NB & SATA RAID & 1394 & SPIO & BIOS
PCIRST#2	MS7	PCI slot 1-2 & PCIE 1-2
HDRST#	MS7	Primary, Scondary IDE

# CPU SIGNAL BLOCK





0	TEJ/PSC
1	RSVD

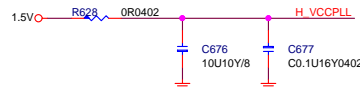
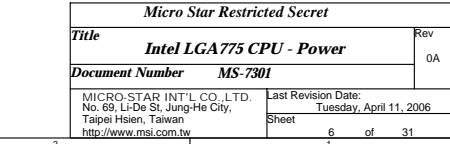
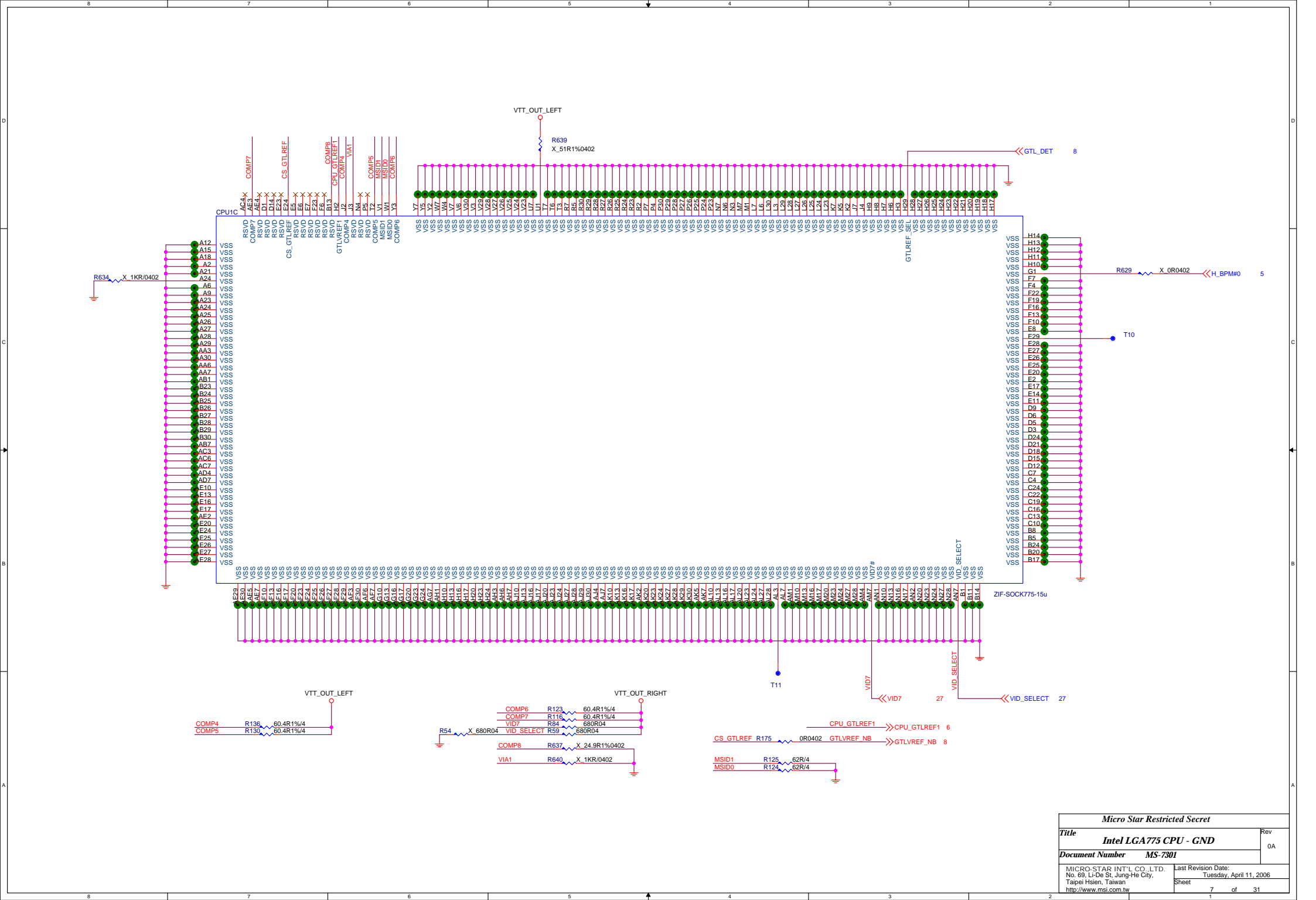


Figure 10 shows the pin connections for the 8P4R-62R/4 connector. The connector has 8 pins. Pins 1, 3, 5, 7, and 8 are connected to V\_FSB\_VTT. Pins 2, 4, 6, and 8 are connected to FERR# and HIERR# signals. The connector is labeled 8P4R-62R/4.

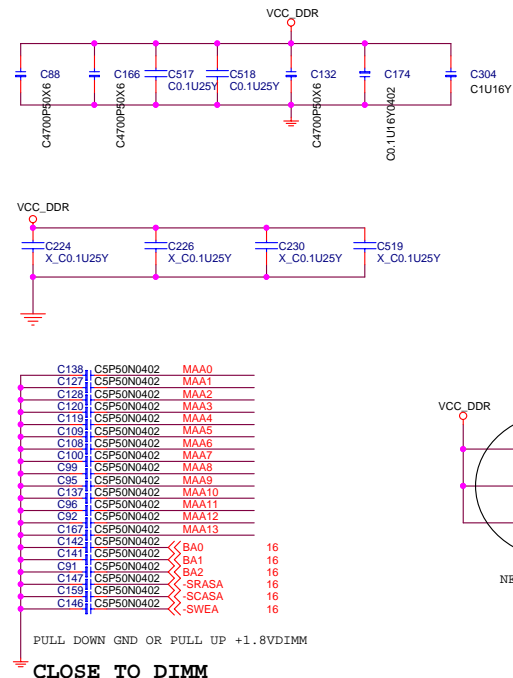
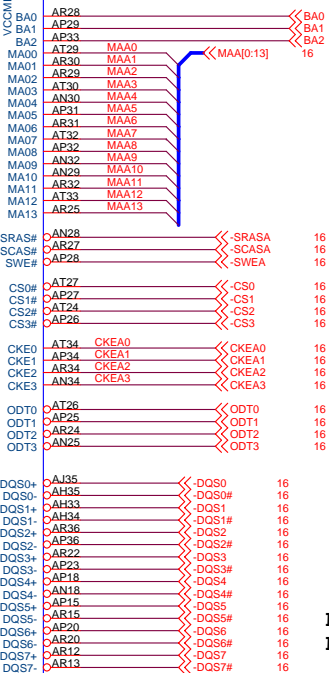
Pin connection diagram for the 8P4R-470R/4 component. The diagram shows a 7-pin connector with pins 1 through 7. Pin 1 is connected to V\_FSB\_VTT. Pin 2 is labeled BSEL2. Pin 3 is labeled BSEL0. Pin 4 is labeled BSEL0. Pin 5 is labeled BSEL1. Pin 6 is labeled BSEL1. Pin 7 is labeled BSEL1. The component is labeled RN20 and 8P4R-470R/4.





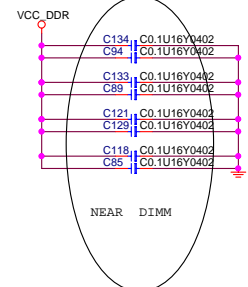
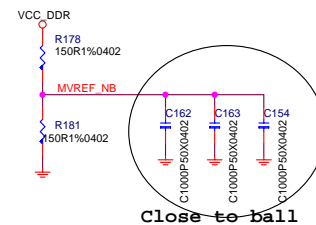


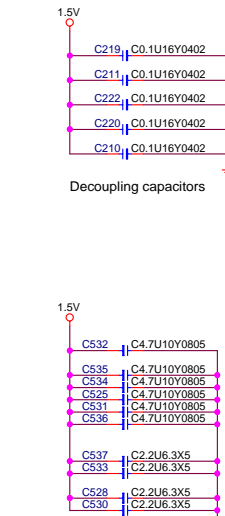
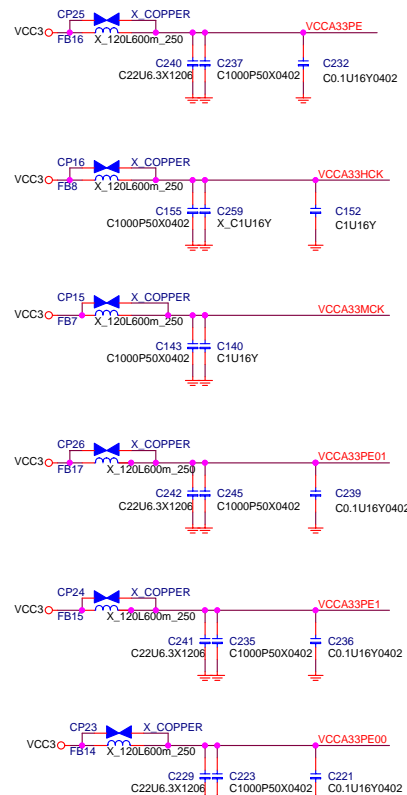




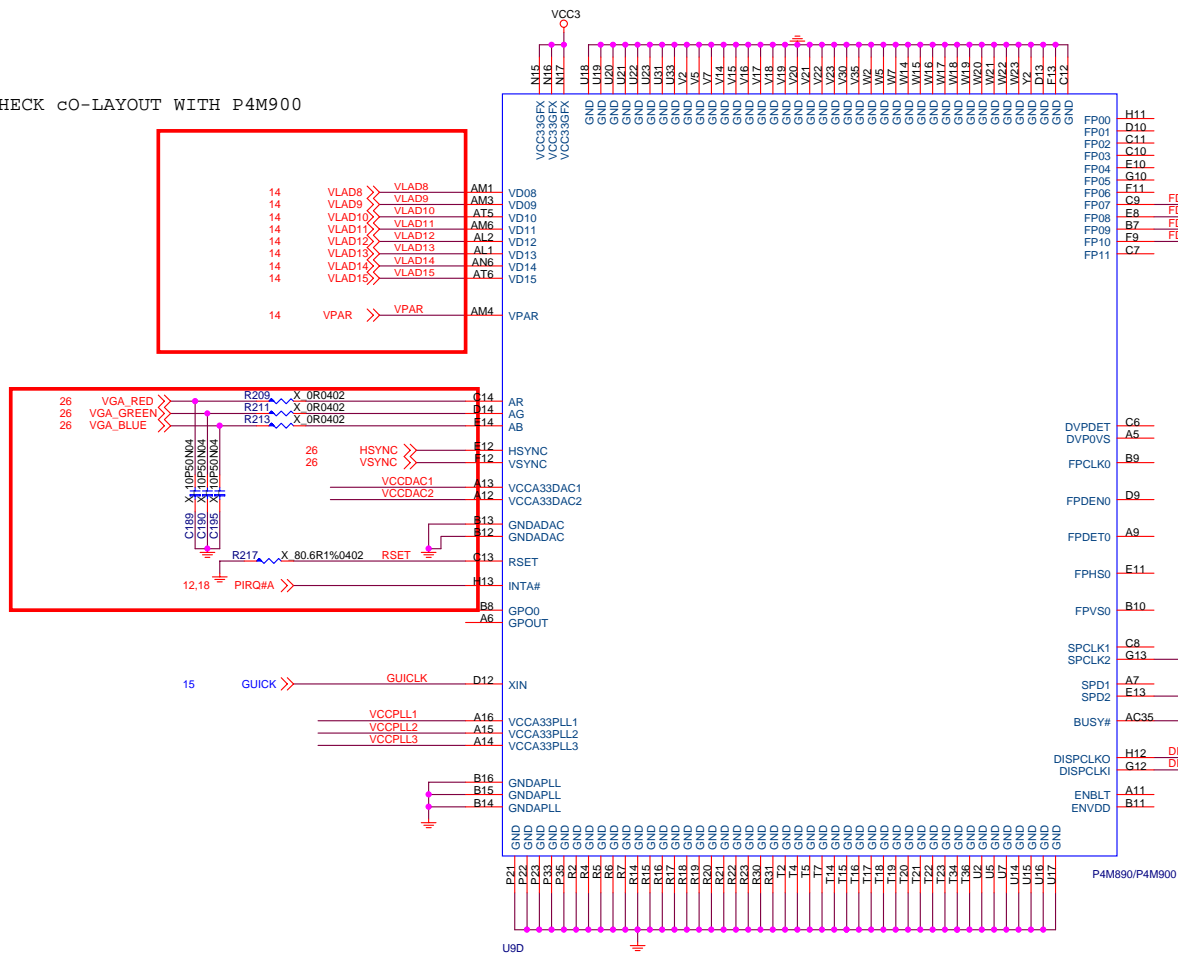
NOTE: DQS/DQS# => OTHER:W:S:W:OTHER=15:10:5:10:15

MCLKO+/- as short as passable  
MCLKIT = DCLKx + 2 "



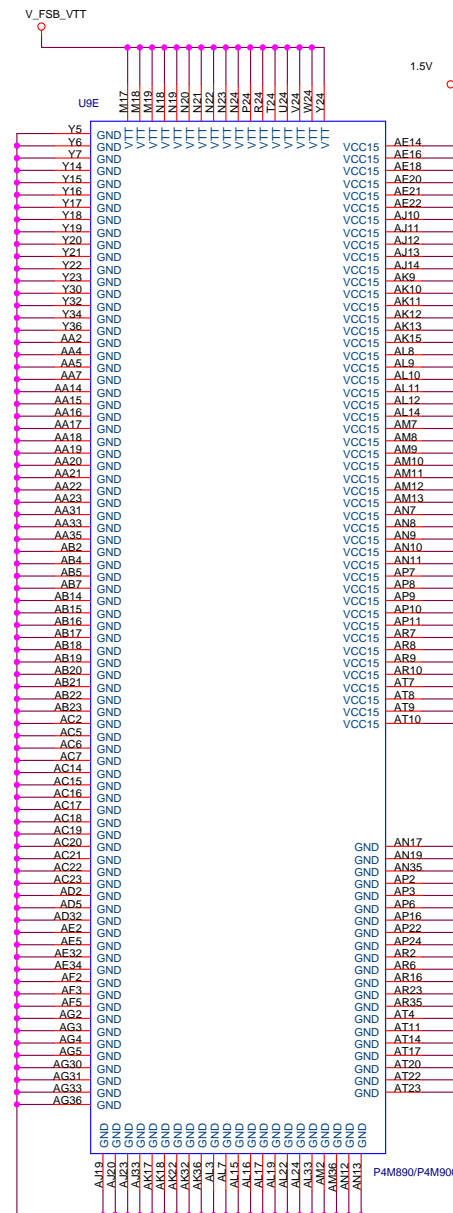
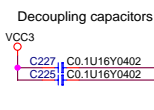
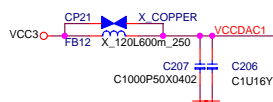
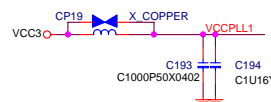
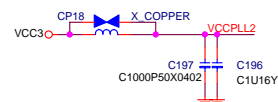
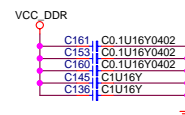
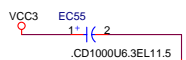
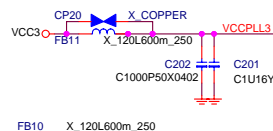
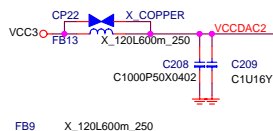


CHECK CO-LAYOUT WITH P4M900

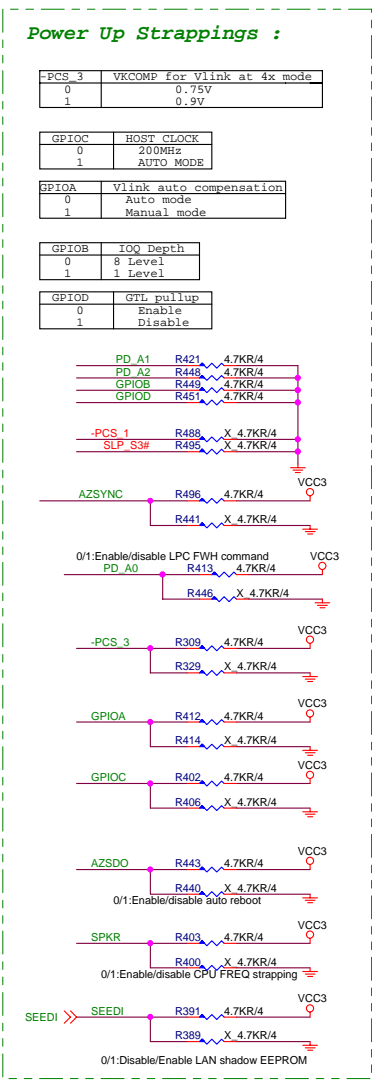


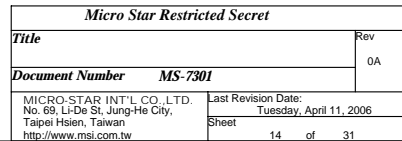
```
FD4 1: 24bit / 0.2 x 12 bit DVI interface
FD5 Dedicated DVI port configuration 0:TMSD 1:TV-encoder
FD6 Dedicated DVI port 0:disable 1:enable
FD7 GFX clock select (VCK/LCDCK/SCK) 0:refer internal PLL 1:from external
FD10 CPUCLK/MCK clock select 0:from NB 1:from external

FD[0:1:2:3:8:9:11] Reserved
```



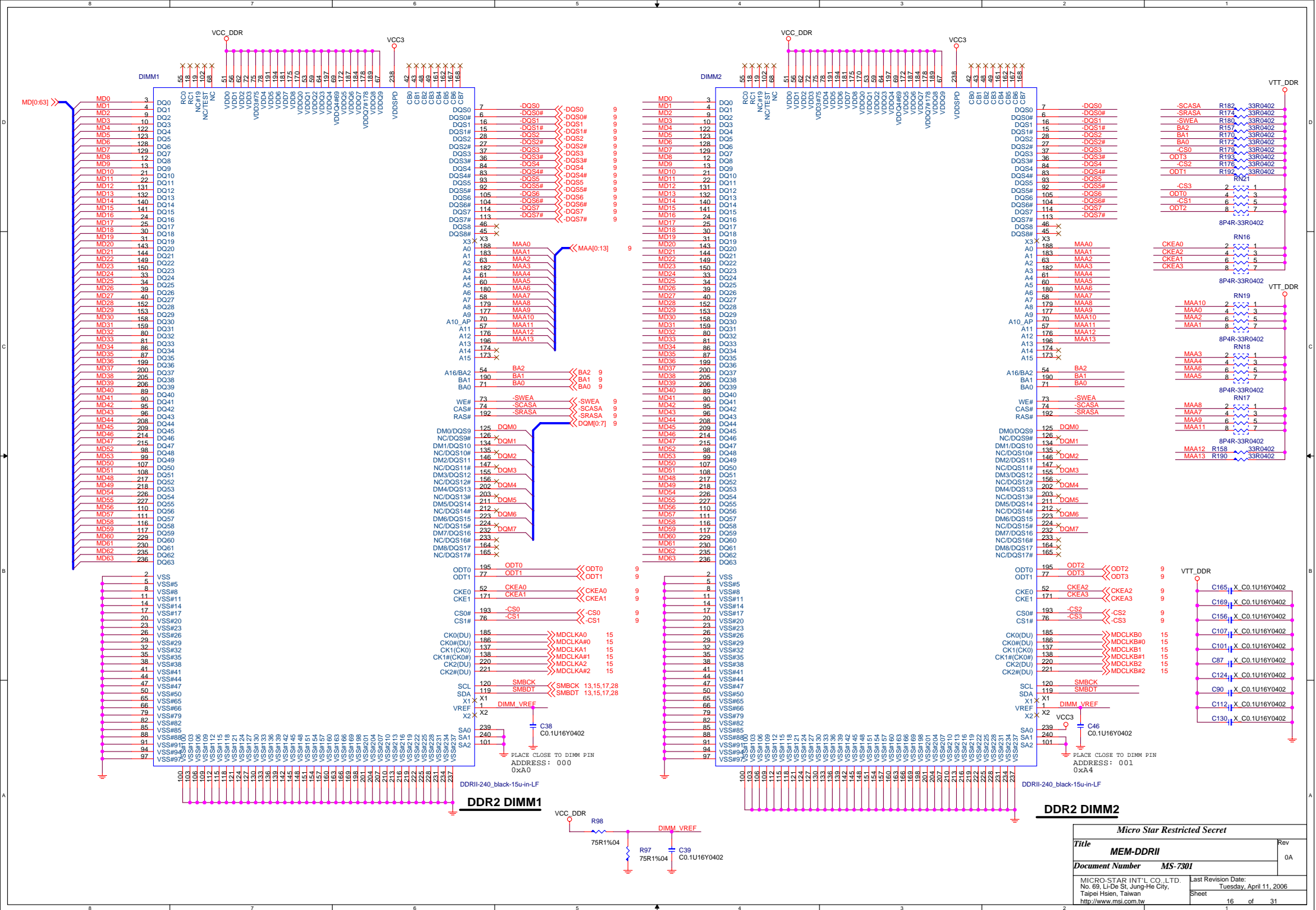




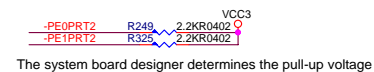






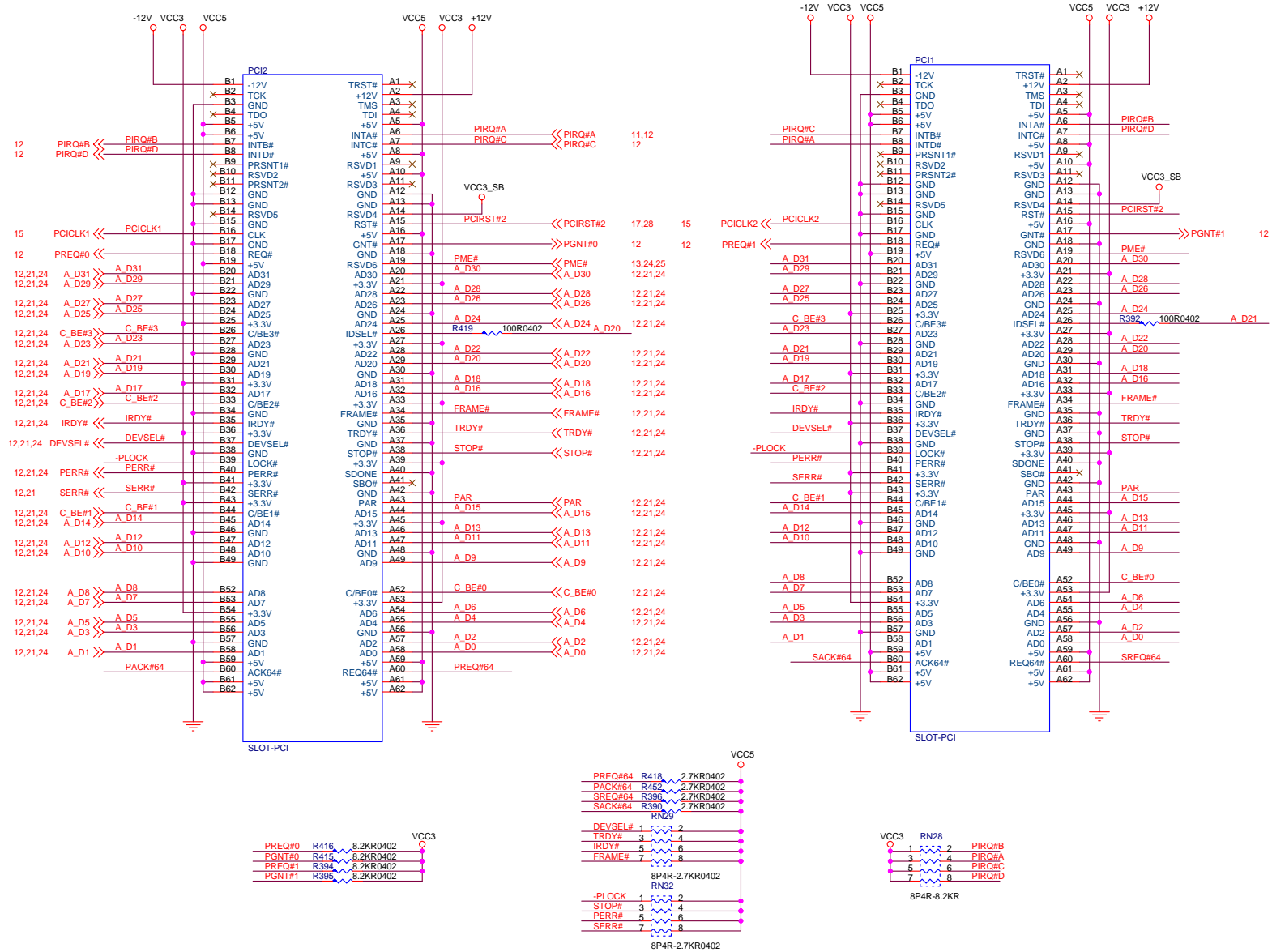




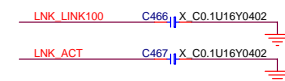
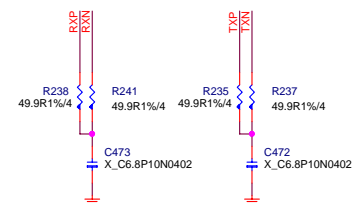
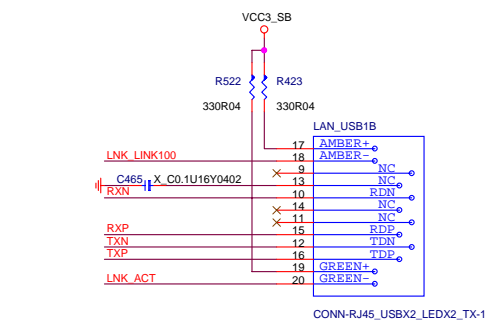
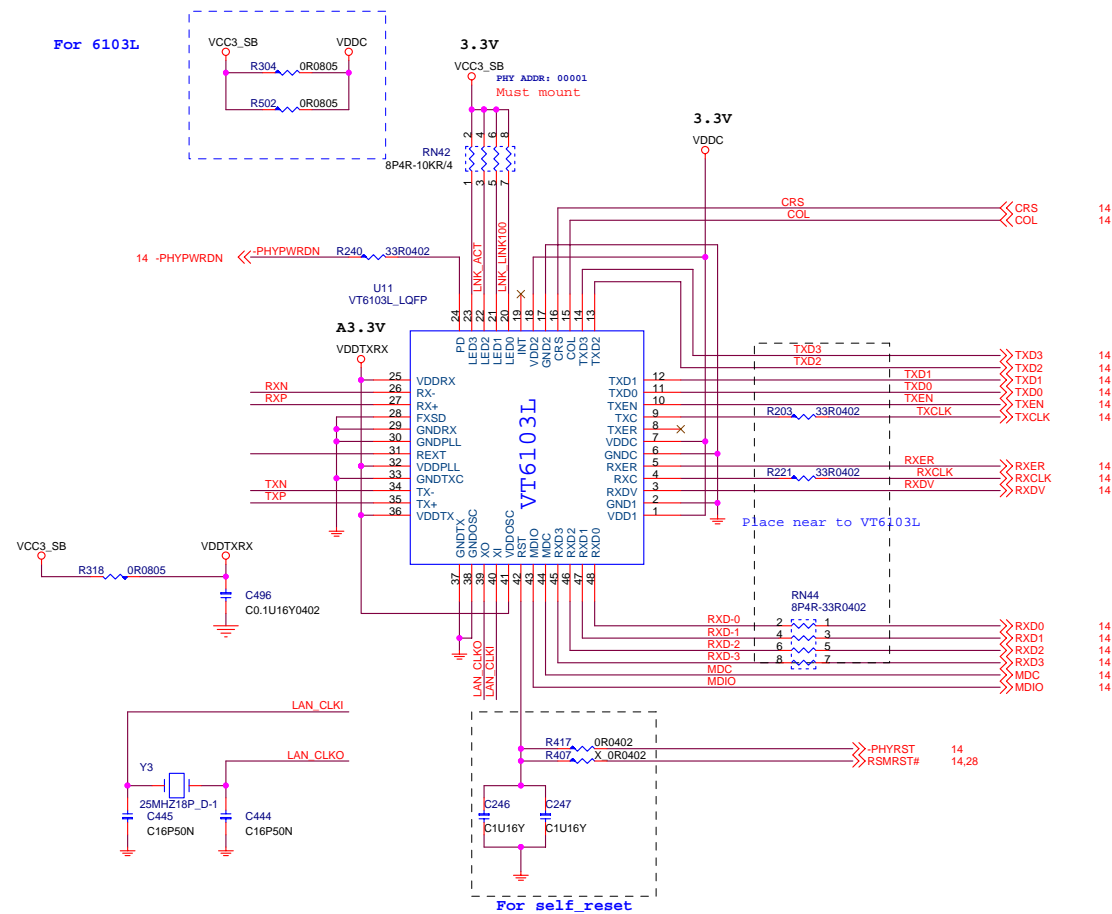


<b><i>Micro Star Restricted Secret</i></b>			
<b><i>Title</i></b> <b><i>PCI-EXPRESS SLOT X16 &amp; X1</i></b>			<b><i>Rev</i></b>
<b><i>Document Number</i></b> <b><i>MS-7301</i></b>			0A
MICRO STAR INT'L CO., LTD. No. 69, Li-De St, Jung-Hsi City, Taipei Hsien, Taiwan <a href="http://www.msi.com.tw">http://www.msi.com.tw</a>		<b><i>Last Revision Date:</i></b> <b><i>Tuesday, April 11, 2006</i></b> <b><i>Sheet</i></b> 17 of 31	

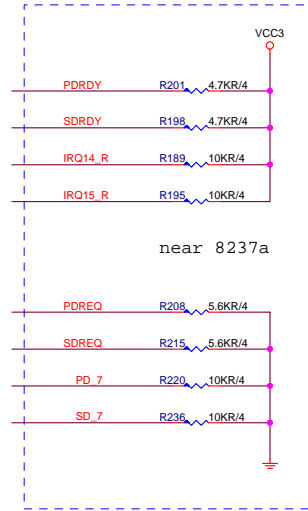
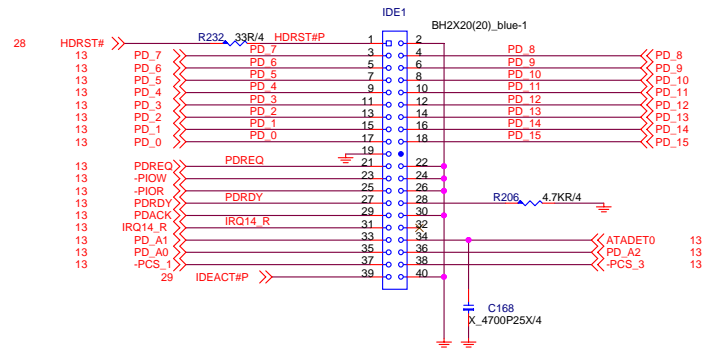
## PCI Connectors



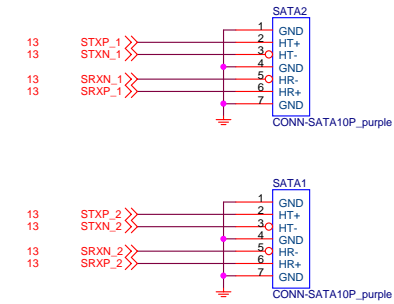




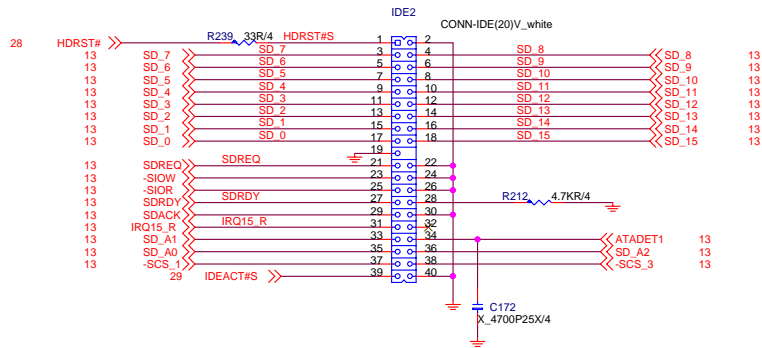
## PRIMARY IDE BLOCK



## SERIAL ATA CONNECTOR BLOCK

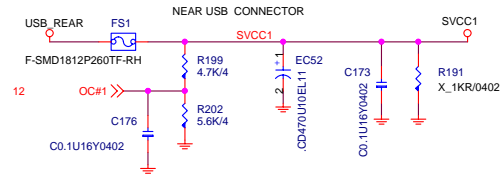


## SECONDARY IDE BLOCK

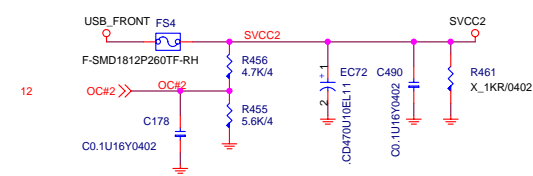


Micro Star Restricted Secret		
Title	IDE & SATA	Rev
Document Number	MS-7301	0A
MICRO-STAR INT'L CO., LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Tuesday, April 11, 2006
Sheet		22 of 31

## POWER CIRCUIT FOR USB PORT 0,1,2,3 (REAR)

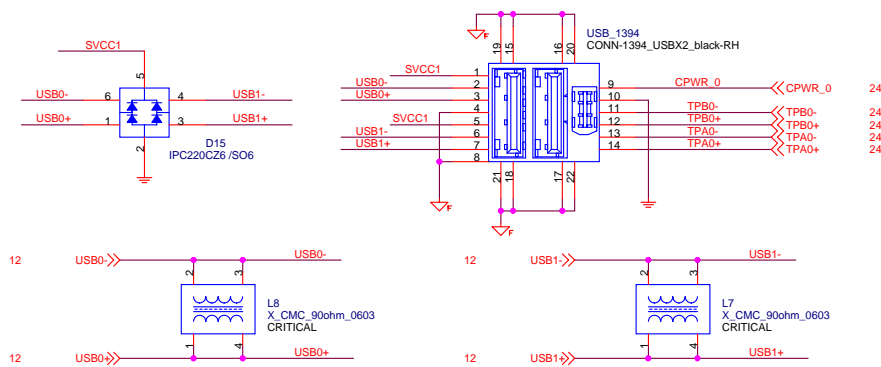


## POWER CIRCUIT FOR USB PORT 4,5,6,7 (FRONT)

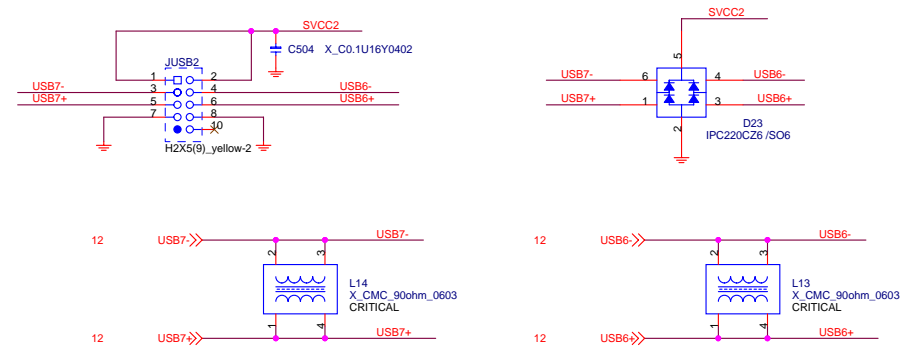


## REAR PANEL USB CONNECTOR FOR USB PORT 0,1 & 1394 PORT

USB Interface  
Diff. Trace width 7.5 mils & 7.5 mils space.  
Diff. & other space 20 mils.  
Length matching: < 150 mils  
Ttrace length 0" to 17"

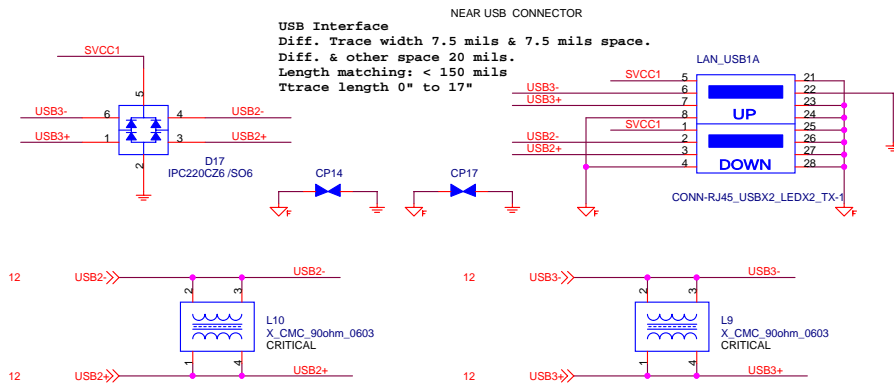


## FRONT PANEL USB CONNECTOR FOR USB PORT 6,7

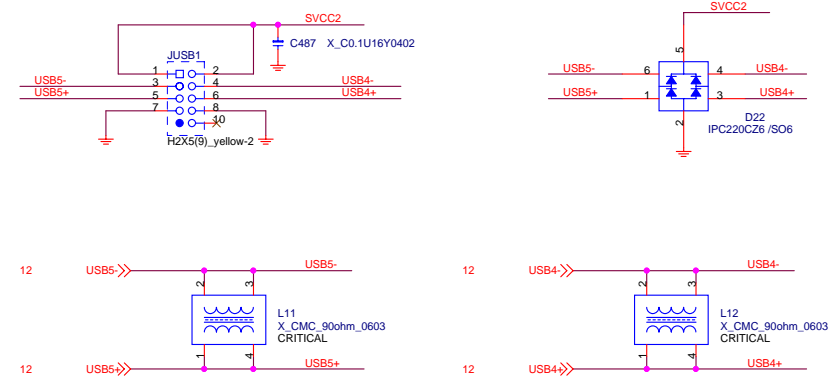


## REAR PANEL USB CONNECTOR FOR USB PORT 2,3

USB Interface  
Diff. Trace width 7.5 mils & 7.5 mils space.  
Diff. & other space 20 mils.  
Length matching: < 150 mils  
Ttrace length 0" to 17"

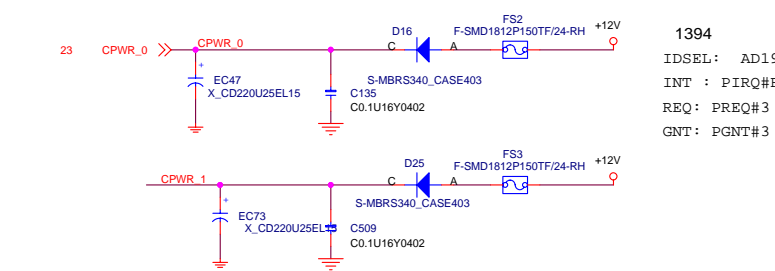


## FRONT PANEL USB CONNECTOR FOR USB PORT 4,5

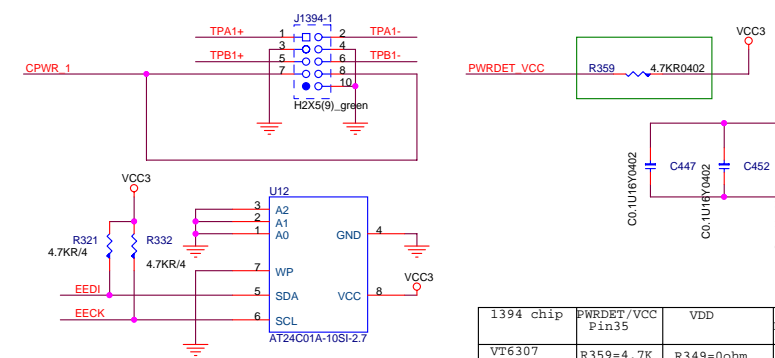
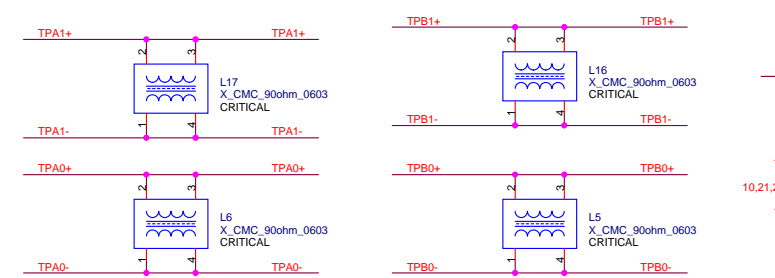
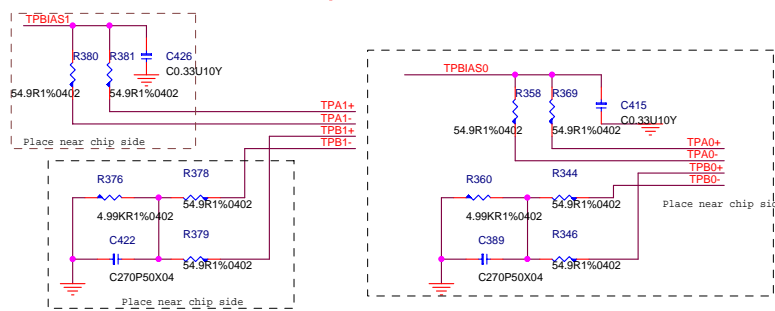


Micro Star Restricted Secret

Title		Rev
USB-REAR & FRONT		0A
Document Number	MS-7301	
MICRO-STAR INT'L CO., LTD. No. 69, Li-De St, Jung-Ho City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Tuesday, April 11, 2006 Sheet 23 of 31



1394  
 IDSEL: AD19  
 INT: PIRQ#F  
 REQ: PREQ#3  
 GNT: PGNT#3



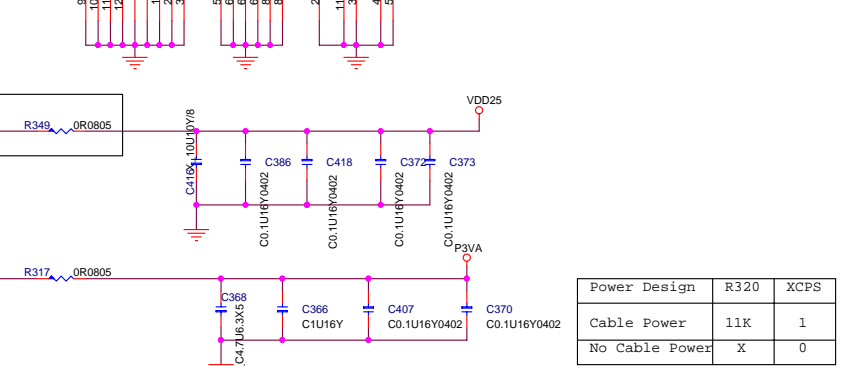
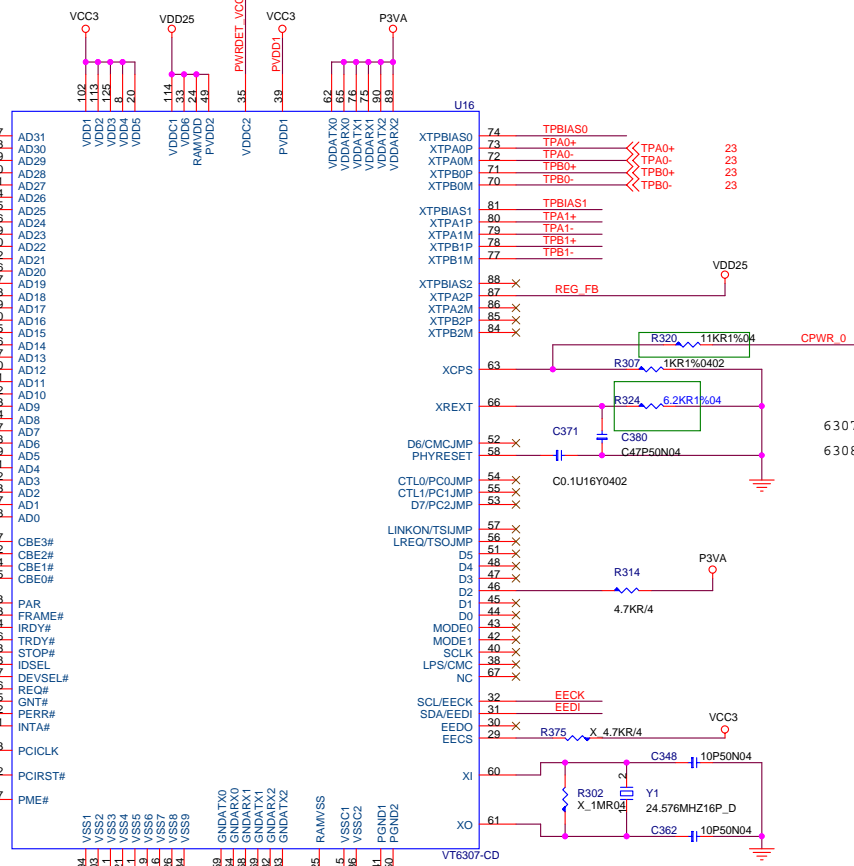
1394 chip	PWRDET/VCC Pin35	VDD	BJT_CTL Enable (R216)	Bandgap resistor R603
VT6307	R359=4.7K	R349=0ohm	No Stuff	6.20K
VT6308P	R359=0ohm	r349 no stuff	No Stuff	6.20K

12,18,21	A_D31	A_D31	97
12,18,21	A_D30	A_D29	98
12,18,21	A_D29	A_D28	99
12,18,21	A_D28	A_D27	100
12,18,21	A_D27	A_D26	101
12,18,21	A_D26	A_D25	102
12,18,21	A_D25	A_D24	103
12,18,21	A_D24	A_D23	104
12,18,21	A_D23	A_D22	105
12,18,21	A_D22	A_D21	106
12,18,21	A_D21	A_D20	107
12,18,21	A_D20	A_D19	108
12,18,21	A_D19	A_D18	109
12,18,21	A_D18	A_D17	110
12,18,21	A_D17	A_D16	111
12,18,21	A_D16	A_D15	112
12,18,21	A_D15	A_D14	113
12,18,21	A_D14	A_D13	114
12,18,21	A_D13	A_D12	115
12,18,21	A_D12	A_D11	116
12,18,21	A_D11	A_D10	117
12,18,21	A_D10	A_D9	118
12,18,21	A_D9	A_D8	119
12,18,21	A_D8	A_D7	120
12,18,21	A_D7	A_D6	121
12,18,21	A_D6	A_D5	122
12,18,21	A_D5	A_D4	123
12,18,21	A_D4	A_D3	124
12,18,21	A_D3	A_D2	125
12,18,21	A_D2	A_D1	126
12,18,21	A_D1	A_D0	127

12,18,21	C_BE#3	C_BE#3	107
12,18,21	C_BE#2	C_BE#2	108
12,18,21	C_BE#1	C_BE#1	109
12,18,21	C_BE#0	C_BE#0	110

12,18,21	PAR	PAR	3
12,18,21	FRAME#	FRAME#	123
12,18,21	IRDY#	IRDY#	124
12,18,21	TRDY#	TRDY#	125
12,18,21	STOP#	STOP#	126
12,18,21	DEVSEL#	DEVSEL#	127
12,18,21	PREQ#3	PREQ#3	96
12,18,21	PGNT#3	PGNT#3	95
12,18,21	PERR#	PERR#	2
12,18,21	PIRQ#F	PIRQ#F	91

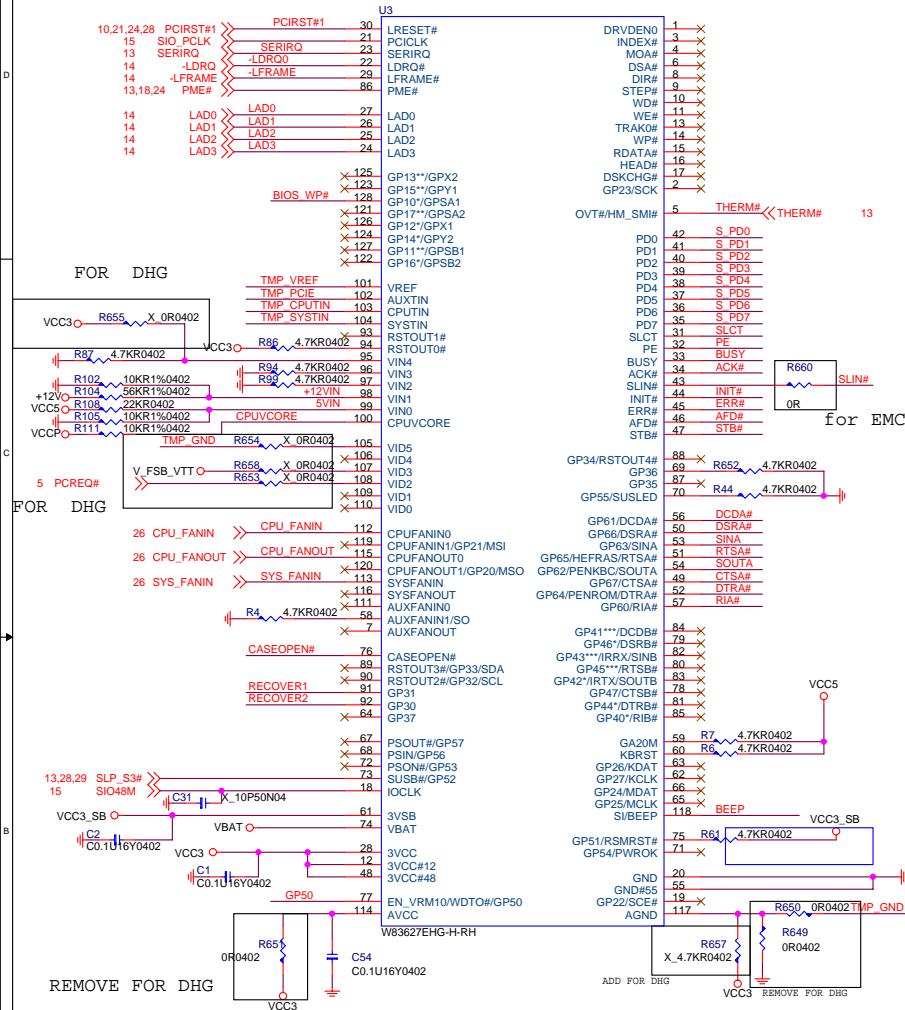
15	1394_PCLK	93
10,21,25,28	PCIRST#1	92
13,18,25	PME#	37



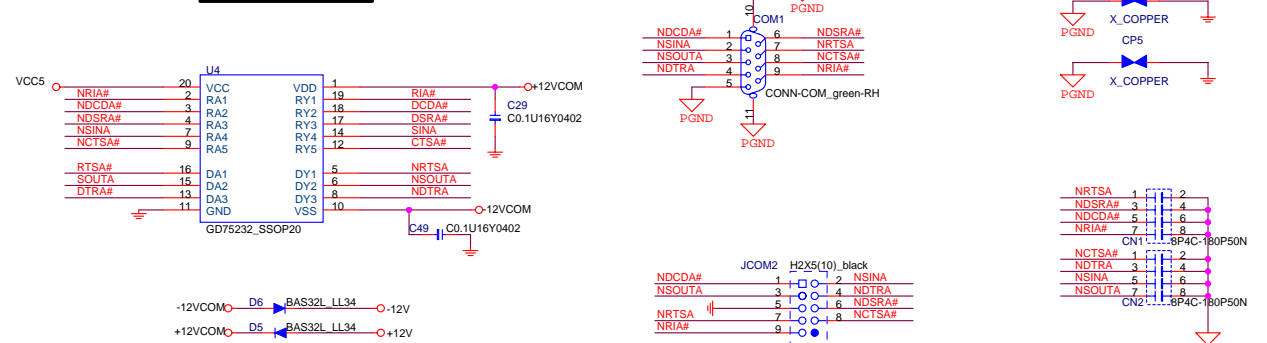
Power Design	R320	XCPS
Cable Power	11K	1
No Cable Power	X	0

## LPC I/O STRAPPING RESISTOR

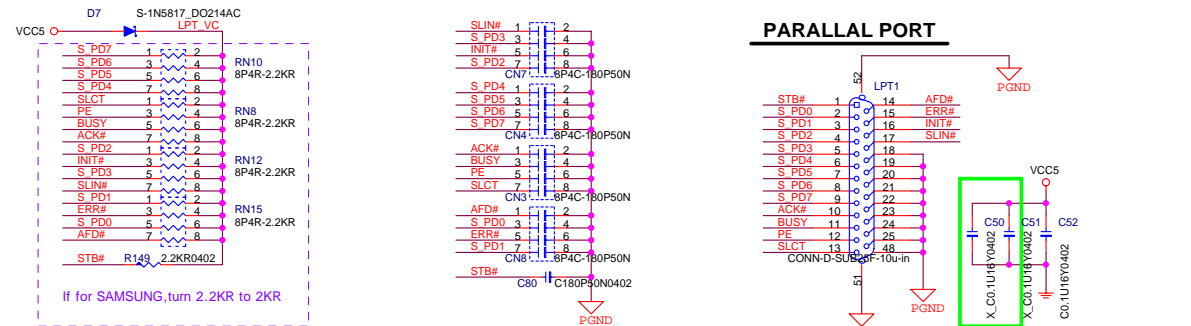
SOUTA	L: Disable KBC	H: Enable KBC
GP50	L: TTL LEVEL	H: VRM10 LEVEL
RTSA#	L: CFAD=2E	H: CFAD=4E
DTRA#	L: PNP Default	H: PNP no Default



## SERIAL PORT 1

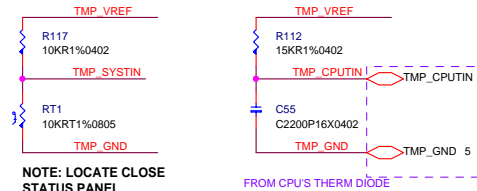


## PARALLAL PORT

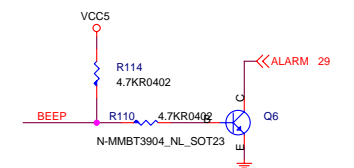


## Temperature Sensing

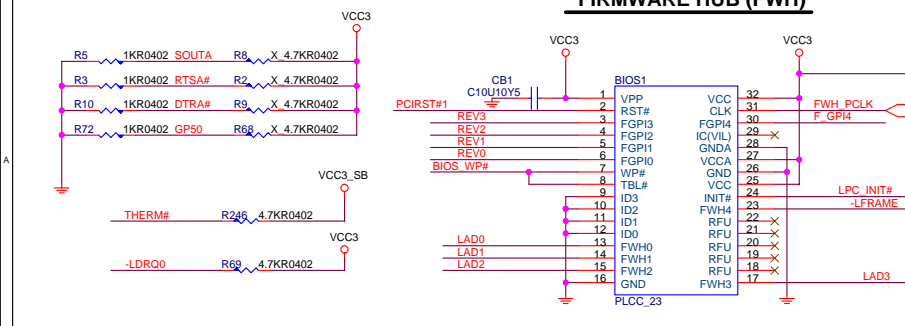
W83627EHF VREF=2.048V



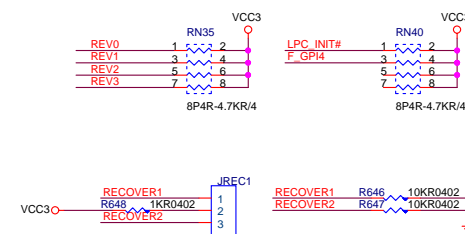
## buzzer control



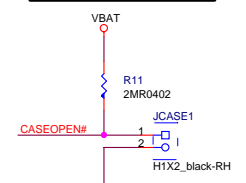
## FIRMWARE HUB (FWH)



## FWH RESISTORS



### Chassis Intrusion



*Micro Star Restricted Secret*

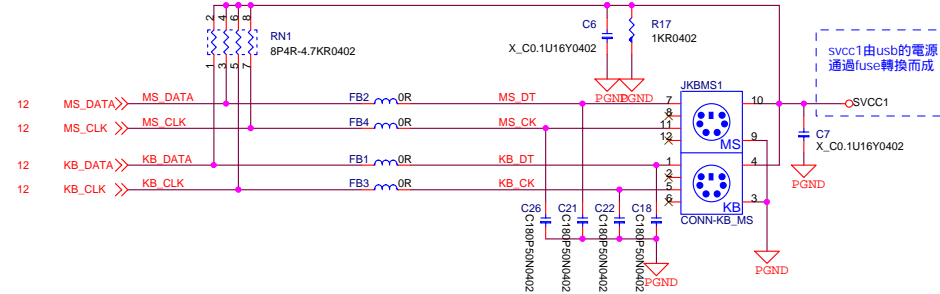
Title	<b>LPC IO-W83627EHG &amp; BIOS</b>
-------	------------------------------------

<b>Document Number</b>	<b>MS-7301</b>
------------------------	----------------

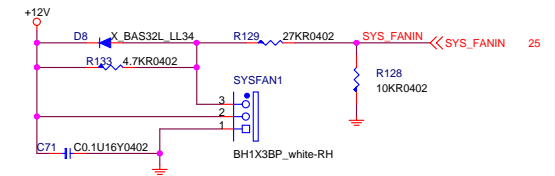
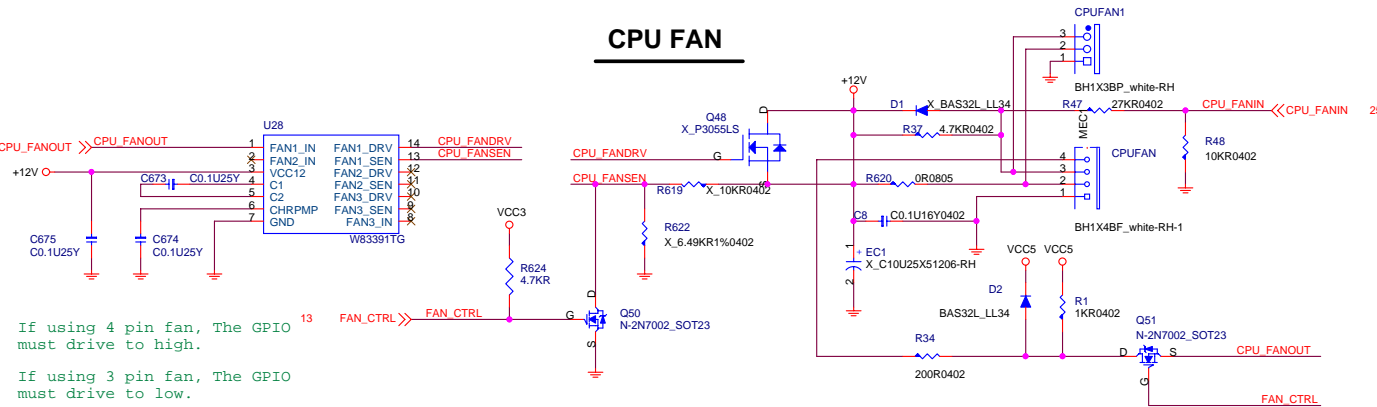
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan <a href="http://www.msi.com.tw">http://www.msi.com.tw</a>	Last Revision Date: Tuesday, April 11, 2006 Sheet 25 of 31
---	---



Fan	Description
Pin 1	GND
Pin 2	POWER
Pin 3	Taco
Pin 4	PWM

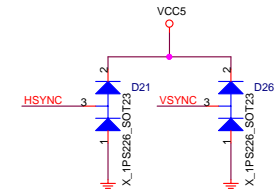


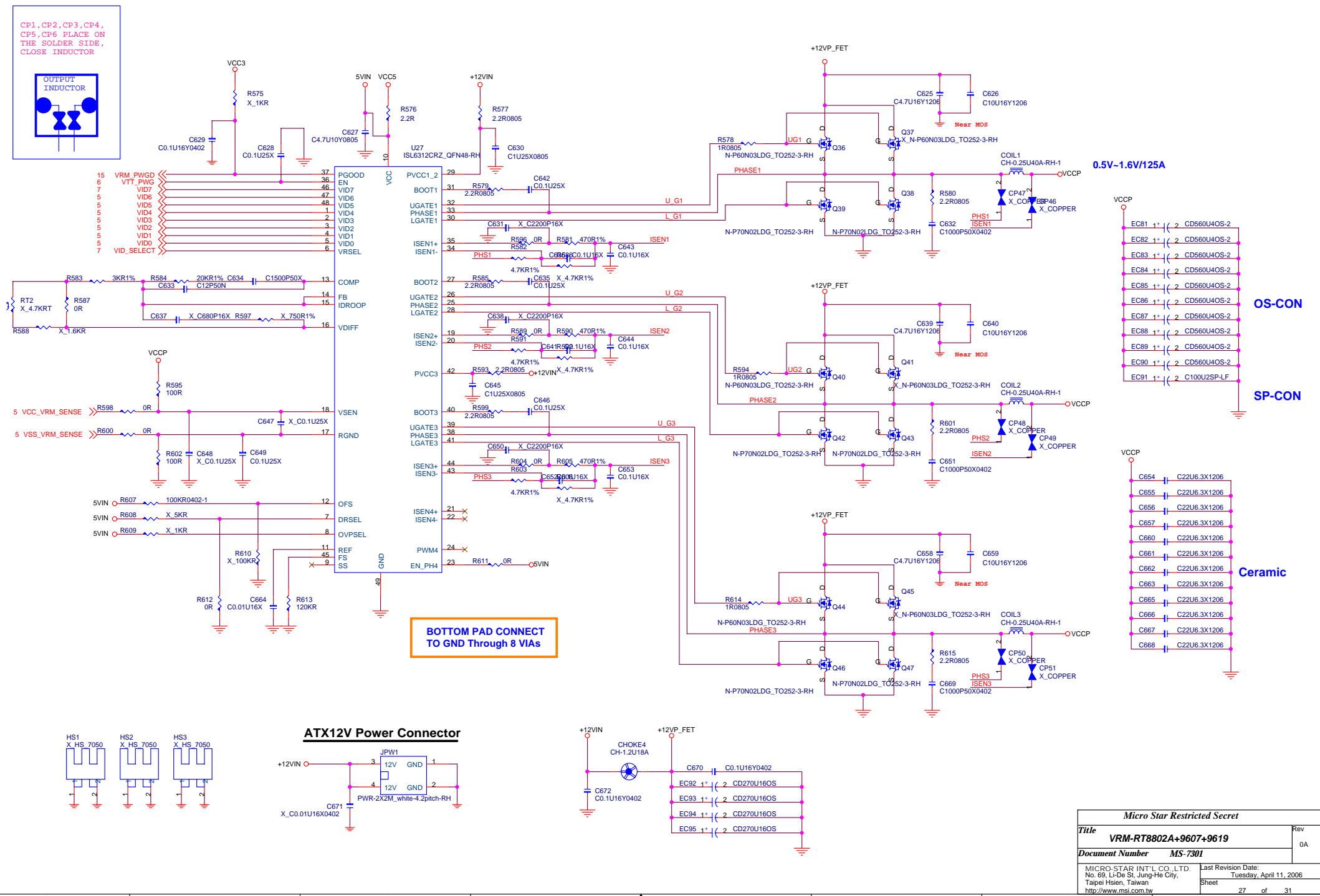
## SYSTEM FAN



# Video Connector

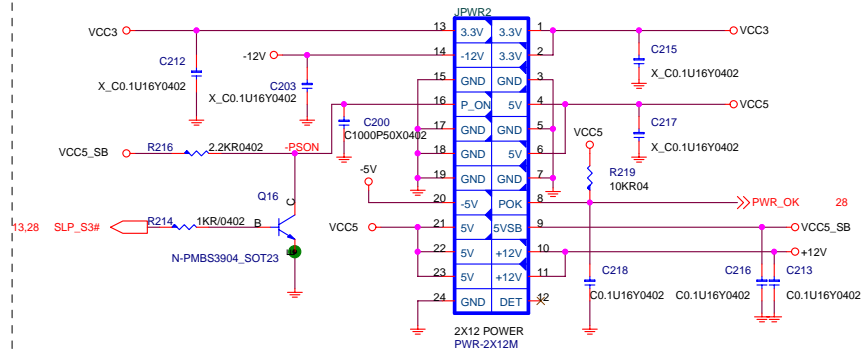
The schematic diagram illustrates the internal wiring of a video connector. It features three main signal paths: VGA (Red, Green, Blue), SPD (Serial Data), and SCLK (Serial Clock). The VGA signals are connected to a 15-pin D-sub connector (X\_CONN-D-SUB15F\_blue-RH-3) via a series of resistors (R156, R157, R158) and capacitors (C123, C124, C125). The SPD and SCLK signals are connected to a 15-pin D-sub connector (X\_CONN-D-SUB15F\_blue-RH-3) via a series of resistors (R159, R160, R161) and capacitors (C126, C127, C128). The diagram also shows a power supply section with a 5V regulator (X\_F-MICROSMD110F-RH) and a ground connection (X\_C0.1U16Y0402). The connector is labeled with pin numbers 1 through 15. The diagram is titled "Video Connector" in a large, bold font.



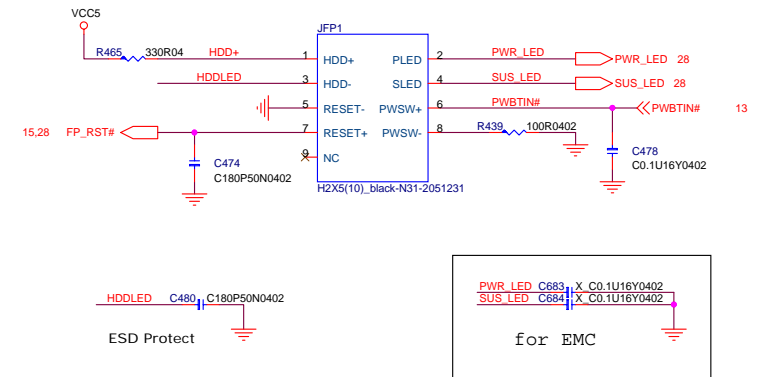




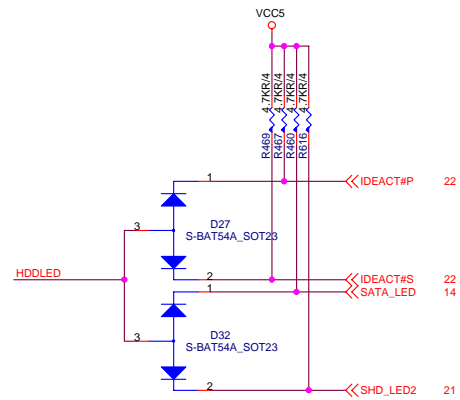
## ATX Connector



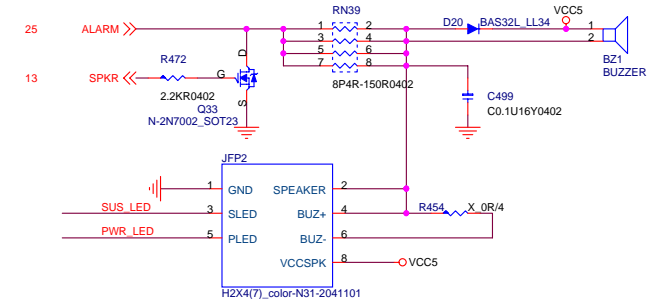
## For MSI / Intel Front Panel



## IDE LED & SERIAL ATA LED

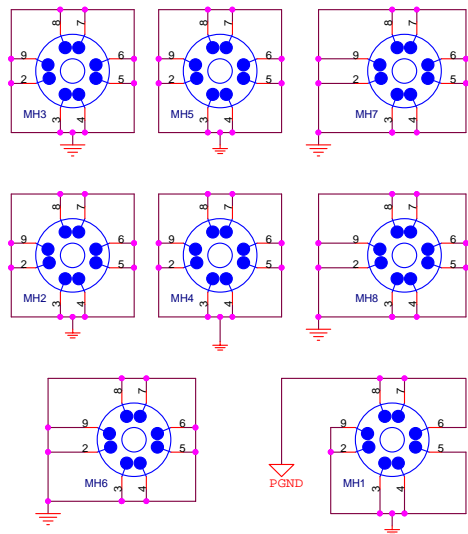
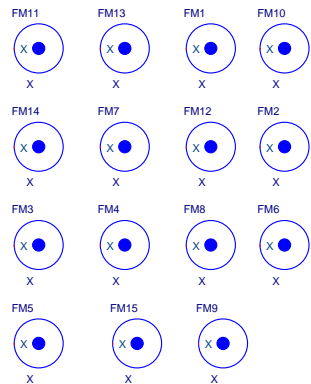


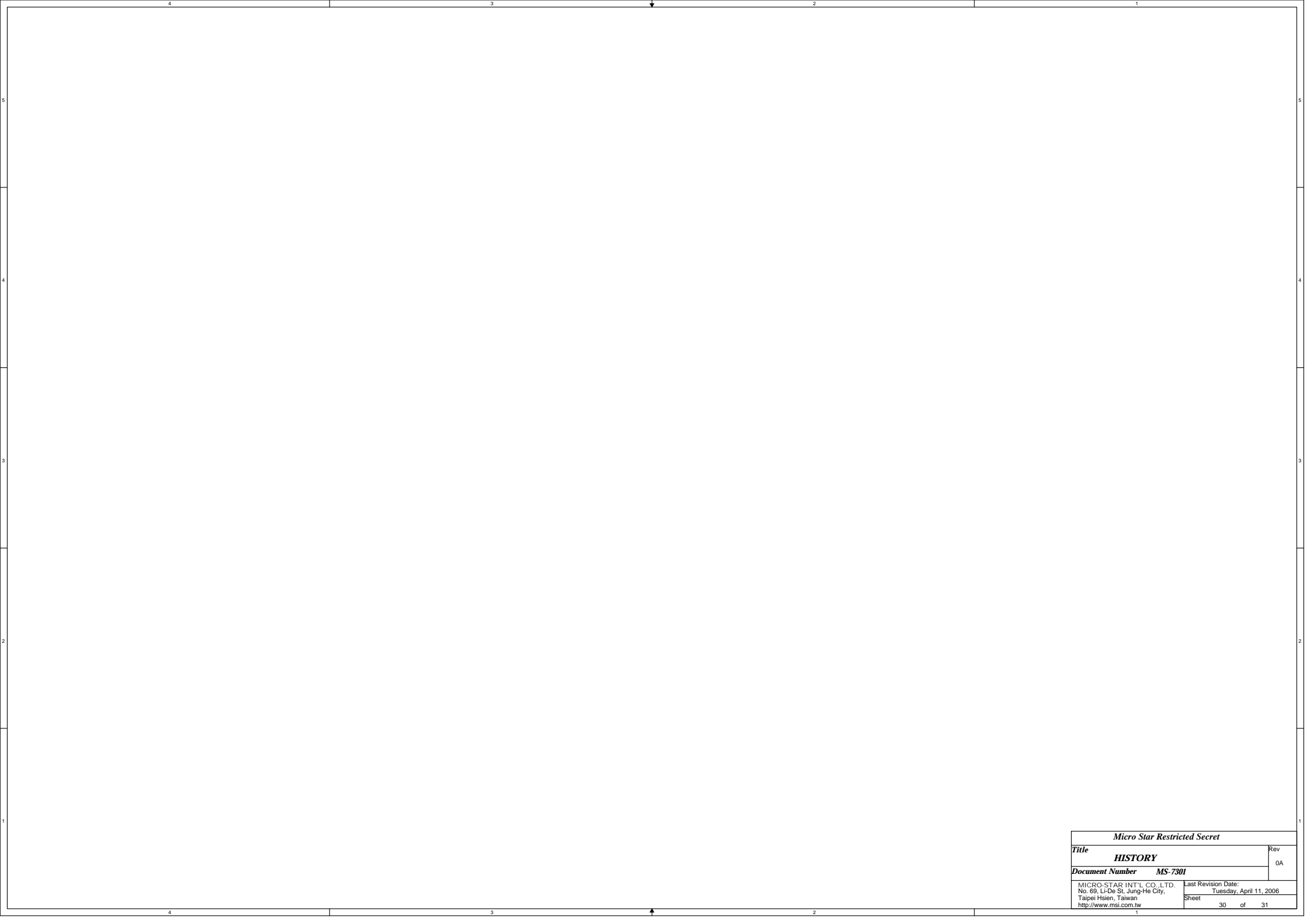
## BUZZER



## For EMI

### Impedance Test





Micro Star Restricted Secret		
Title	HISTORY	Rev 0A
Document Number	MS-7301	
MICRO-STAR INT'L CO. LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan <a href="http://www.msi.com.tw">http://www.msi.com.tw</a>		Last Revision Date: Tuesday, April 11, 2006
Sheet		30 of 31